REMARKS

Upon entry of the instant Amendment, Claims 1-10, 12, 14, and 19-20 are pending. Claims 16-18 have been canceled. Claim 14 has been amended to correct a typographical error.

Claims 1-10, 12, 14, and 16-20 have been rejected under 35 U.S.C. 103 as being unpatentable over Paradine et al., U.S. Patent No. 6,049,565 ("Paradine") in view of Hirata, U.S. Patent No. 5,327,391 ("Hirata"). Applicants respectfully submit that the claimed invention is not taught, suggested or implied by Hirata or Paradine, either singly or in combination.

As discussed in the Specification, the present invention relates to a system and method for rate adjustment.

A rate adjustment system according to an embodiment of the invention includes a first jitter buffer pair and a second buffer pair. The buffers in the first and second jitter buffer pairs are swapped to effect a rate adjustment. In particular, the buffers in the pairs are alternately filled at a first clock rate and emptied at a second. The swapping occurs at the second clock rate.

Thus, claim 1 recites "wherein said first or second jitter buffers alternately fill at said first clock frequency and empty at said second clock frequency, and said third or fourth jitter buffers alternately fill at said second clock frequency and empty at said first clock frequency, wherein alternation between said first and second jitter buffers and said third and fourth jitter buffers occurs at said second clocking frequency;" claim 5 recites "wherein said first or second jitter buffers alternately fill at a first clock frequency and empty at a second clock frequency, wherein alternation between said first and second jitter buffers occurs at said second clock frequency; and wherein said third or fourth jitter buffers alternately fill at said second clock frequency and empty at said first clock frequency, wherein alternation between said third and fourth jitter buffers occurs at said second clock frequency;" claim 12 recites said first and second jitter buffers adapted to receive a plurality of samples at a first clock rate and transmit a block of said samples at a second clock rate, and further including third and fourth jitter buffers,

adapted to receive blocks of samples at said second clock rate and transmit a plurality of samples at said first clock rate, the method comprising: switching between using said first or second jitter buffers at said second clock rate; and switching between using said third or fourth jitter buffers at said second clock rate;" claim 14 recites "receiving at first or second jitter buffers a plurality of samples at a first clock rate and transmitting a block of said samples at a second clock rate; and switching between using said first or second jitter buffers at said second clock rate; and receiving at third or fourth jitter buffers blocks of samples at said second clock rate and transmitting a plurality of samples at said first clock rate; and switching between using said third or fourth jitter buffers at said second clock rate;" and claim 19 recites first and second pairs of jitter buffers interfacing between said first circuitry and said second circuitry domain; wherein ones of said pairs of first or second jitter buffers are swapped according to a clock by which said ones of said pairs of first or second jitter buffers are filled or emptied."

In contrast, contrary to the suggestion in the Official Action, Paradine has nothing to do with swapping buffers. While Paradine provides a double buffer 320 and a double buffer 330, the halves of the double buffers are never swapped. Instead, samples are passed into one half of the buffer and read out of the other. No swapping of halves occurs.

Hirata similarly fails to disclose switching individual ones of pairs of buffers according to a same frequency, as generally recited in the claims at issue. As discussed above, according to embodiments of the present invention, one pair of buffers operates in a first "direction" and the other operates in a second "direction." That is, the first pair is filled at a first clock and emptied at a second clock rate. The second pair is filled at the second clock rate and emptied at the first. The individual buffers in the pairs are swapped at the second clock rate. Thus, both oppositely directed pairs are swapped according to the same clock rate.

In contrast, Hirata provides a first data memory 24-1 and a second data memory 24-2. Usage of the first and second data memories is governed by selector 23. First generating circuit 21 provides input to write in counters 25-1 and 25-2 and 2nd signal generating circuit provides input to read-out counters 26-1 and 26-2. Nevertheless, Hirata nowhere provides for oppositely directed pairs of jitter buffers to be swapped at a

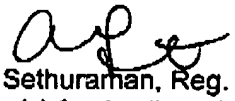
common clock rate. Hirata is merely unidirectional. Thus, even if combined with Paradine, the result would be different selectors operating in *different* clock domains. That is, the selection of buffers would be done at different clocks, as opposed to the present invention, in which swapping occurs at a same clock rate. As such, the Examiner is respectfully requested to reconsider and withdraw the rejection of the claims.

For all of the above reasons, Applicants respectfully submit that the application is in condition for allowance, which allowance is earnestly solicited.

PLEASE MAIL CORRESPONDENCE TO:

Siemens Corporation
Customer No. 28524
Attn: Elsa Keller, Legal Administrator
170 Wood Avenue South
Iselin, NJ 08830

Respectfully submitted,



Anand Sethuraman, Reg. No. 43,351
Attorney(s) for Applicant(s)
Telephone: 650-943-7554
Date: 3/9/06